extending to a conductive region extending below said pillar.

20. (Amended) A transistor as recited in claim 18, wherein said gate structure extends on two sides of said channel.

35. A transistor as recited in claim 34 wherein said substrate comprises SOI having buried oxide isolation and wherein said insulation comprises said buried oxide isolation.

REMARKS

Claims 1 - 44 remain active in this application. Claims 11 - 17 have been withdrawn from consideration as being non-elected, with traverse, in response to a requirement for restriction. The specification has been reviewed and editorial revisions made where seen to be appropriate. Claims 2, 3, 6, 8, 20 and 35 have been amended to improve form. No new matter has been introduced into the application.

It is noted with appreciation that the requirement for restriction has been modified in view of the previously submitted traverse and the requirement, as modified, has been made final. No further traverse is presented. However, the non-elected claims 11 - 17 are retained in this application but will be canceled when a divisional application is filed.

It is also noted for the record that no rejection or objection is applied to many claims in the application other than a blanket rejection of all claims under 35 U.S.C. §112, second paragraph which is clearly in error as will be discussed below. Since an official action should be complete in all particulars, it is assumed that claims 20 - 24, 29 - 31, 33, 34, 36, 37 and 41 - 44 are considered to be directed to

allowable subject matter although not explicitly so indicated by the Examiner. If, however, the action is incomplete, it is respectfully submitted that the next action in this application cannot properly be made final.

The Examiner has objected to the specification in regard to two typographical matters. This objection is respectfully traversed as being moot in view of the amendments made above.

The Examiner has further objected to the specification under MPEP 608.01(o); citing several narrative phrases of the claims for which it is asserted that antecedent language is not provided. This objection is also respectfully traversed.

Initially, it is respectfully pointed out that the cited section of the MPEP is principally directed to terminology and altered terminology inserted by amendment, in particular. The citation of long, narrative phrases rather than particular terms is largely non-informative and places a substantial burden on the Applicant to discern the Examiner's meaning. Further, it is respectfully pointed out that claims form a portion of the disclosure and, to that extent, are self-supporting. However, in an effort to fully respond to the Examiner's criticisms, support for the claim language is listed below.

Claim 3: isolation material surrounding insulation or transistor locations is discussed on pages 5, 9, 15, 19 and 21;

Claim 23: reference to the gate extending on two *or more* sides of the conduction channel appears at page 16, line 6;

Claim 33: a contact between two diffusions extending over an insulator appears at page 21, line 21+;

Claim 34: an etched and deposited isolation structure is discussed at page 15, line 28+;

Claim 35: SOI and formation of isolation buried therein is discussed on pages 17 - 18;

Claim 37: a gate structure completely surrounding the channel is discussed on page 12, line 19;

Claim 38: a gate structure self-aligned with the channel is discussed at page 12, line 7; and

Claim 41: borderless contacts are discussed at many locations including pages 12 - 14 and defined on page 15.

Accordingly, it is respectfully submitted that adequate antecedent terminology is present in the specification for the passages noted by the Examiner. Therefore, reconsideration and withdrawal of this objection is respectfully requested. Should any issue remain, in the Examiner's view, increased specificity of the criticism is respectfully requested.

Claims 2, 3, 6, 8, 20 and 35 have been rejected under 35 U.S.C. §112, second paragraph, as being indefinite. This rejection is respectfully traversed as being moot in view of the amendments made above. All of the criticisms by the Examiner are directed to matters of antecedent language correspondence and, by the above amendments, antecedent language correspondence has been revised and is now believed to be exact. In any event, it is also respectfully submitted that the language of the claims as originally filed did not engender ambiguity or compromise the determination of the scope of any claim. Therefore, it is respectfully requested that this rejection be reconsidered and withdrawn.

Claims 1 - 10 and 18 - 44 have been rejected under 35 U.S.C. §112, second paragraph; the Examiner raising questions in regard to the language "selectively etchable", "borderless" and "sub-lithographic" in enumerated claims. This rejection is also respectfully traversed.

It is respectfully submitted that all of these

terms are well-accepted and recognized terms of art. Further, all relate to the formation of contacts which is an important and distinguishing feature of the present invention. The term "borderless" is defined on page 15 of the specification the provision of a contact to a structure without providing an insulator over the structure by forming a contact opening in or along an existing insulator. A disclosed in copious detail throughout the specification, the invention provides for the formation of such contact openings by selective etching at an interface between two materials that can be selectively etched relative to each other. Silicon oxide and silicon nitride are an exemplary pair of materials noted numerous times in the specification that can be selectively etched relative to each other since etchants are known which provide markedly different etch rates of the two materials. Thus, an opening can be formed in one of the materials along its interface with the other and, if etching is done in accordance with a mask feature of minimum lithographic feature size and overlapping the interface of the two materials, the opening will be smaller than can be resolved by a lithographic exposure and, hence, is "sub-lithographic" in dimensions. Sidewall spacers are another well-known structure which is commonly referred to as sub-lithographic since they are formed without a mask using deposition and etching having different preferential progress directions.

Therefore, since the question language is, in fact, well-recognized and well-understood terminology in the art as well as being explained and/or defined in detail in the disclosure, it is respectfully submitted that no ambiguity or uncertainty of claim scope can be engendered by the criticized/questioned passages. Accordingly, reconsideration and withdrawal of this ground of rejection is respectfully requested.

Claims 1 - 10 have been rejected under 35 U.S.C.

§102 as being anticipated by Alavi; claims 18, 19, 32, 38 and 40 have been rejected under 35 U.S.C. §102 as being anticipated by Malhi et al.; claims 25 and 35 have been rejected under 35 U.S.C. §103 as being unpatentable over Malhi et al. and claims 26 - 28 have been rejected under 35 U.S.C. §103 as being unpatentable over Malhi et al in view of Alavi. All of these grounds of rejection are respectfully traversed since neither Alavi nor Malhi et al. teaches or suggests the particular form of contacts provided in accordance with the invention.

Specifically, while Alavi teaches a vertical MOS structure, the contact openings are formed by lithographic etching of an interlayer dielectric (ILD) layer and not "borderless" by being along existing insulators through selective etching of two insulating materials at their interface. See Figures 24 and 39, column 5, lines 52 - 65 and column 6, lines 33 - 41. Malhi et al. is directed to an entirely different structure forming two transistors of complementary types with a common gate and is essentially irrelevant to the structure claimed. Therefore neither reference can lead to an expectation of success in achieving the meritorious effects of the invention or provide evidence of a level of ordinary skill in the art which would support the Examiner's conclusion of obviousness.

Accordingly, it is respectfully submitted that the Examiner has not made a *prima facie* demonstration of anticipation or obviousness of any claim in the application by failing to address the recitations which support the formation of borderless and sub-lithographic contacts by being selectively etchable or formed at an interface of insulation and isolation structures, as recited in all claims of the application. The Examiner has essentially ignored all such recitations, perhaps through buttressing the rejections with the blanket rejection under 35 U.S.C.

§112 of all claims directed to this feature of the invention, which is, itself, improper. Accordingly, all of the grounds of rejection based on Alavi and/or Malhi et al. are seen to be clearly in error and, upon reconsideration, should be withdrawn.

Since all rejections, objections and requirements contained in the outstanding official action have been fully answered and shown to be in error and/or inapplicable to the present claims, it is respectfully submitted that reconsideration is now in order under the provisions of 37 C.F.R. §1.111(b) and such reconsideration is respectfully requested. Upon reconsideration, it is also respectfully submitted that this application is in condition for allowance and such action is therefore respectfully requested.

If an extension of time is required for this response to be considered as being timely filed, a conditional petition is hereby made for such extension of time. Please charge any deficiencies in fees and credit any overpayment of fees to Deposit Account No. 09-0456 of International Busness Machines corporation (Burlington).

Respectfully submitted,

Marshall M. Curtis
Reg. No. 33,138

APPENDIX

Page 9, line 16+:

Referring now to Figures 5A - 5C, the position of a mold for forming the vertical silicon pillar which will form the vertical conduction channel of the transistor is defined by application of a resist 510. The resist is then exposed using a hard phase shift mask or other lithographic process or other process techniques such as spacers to control width and developed to form a narrow (possibly of sub-lithographic width) linear pattern 520 across the non-STI region. Then, in accordance with the patterned resist, the nitride, GeO_2 and pad oxide are etched selectively to fill 410 to the original silicon wafer surface 620 to form the pillar mold 610, as shown in Figures 6A - 6C, [ande] and the resist stripped. The silicon pillar 710 is then epitaxially and selectively grown from the original silicon wafer surface 620 to fill the mold 610 and the surface planarized to result in the structure shown in Figures 7A - 7C. If pattern 520 is of sub-lithographic width, as can be achieved by, for example, a phase shift mask, the pillar/conduction channel will be of corresponding sub-lithographic dimensions.

Page 12, line 4+:

Then, as shown in Figures 14A - 14C, a sacrificial oxide 1430 is formed on exposed silicon surfaces and stripped. The gate dielectric 1420 is formed self-aligned with the channel by either oxidation or CVD, atomic layer epitaxy or the like that may completely surround the channel. At this point, a heat treatment can be performed to move the out-diffused dopant regions 1410 from the ASG and BSG to form the drain in the lower part of the transistor. This out-diffusion must eventually reach the implanted regions 160, 170,

respectively. The trench 1430 is then filled with a gate material (self-aligned with the channel and gate dielectric) such as polysilicon to create gate electrodes 1440 (Figure 15A - 15C) that are initially joined forming an interior wall completely surrounding the channel but which can be later separated by polishing gate 1440 and residual dopant films such as 1440 that are still present down to nitride 910, recessing the gate material at 1510, and depositing nitride [1530] 1550 in the recess, as shown in Figure 15A - 15C. Then the gate material is further recessed at 1510 and TEOS is deposited and then etched to form sidewall spacers 1520.

Claims 2, 3, 6, 8, 20 and 35:

2. (Amended) A vertical transistor as recited in claim 1, further including isolation material adjacent said layer of [insulating material] insulator and surrounding said vertical transistor, said isolation material being selectively etchable relative to said layer of insulator.

3. (Amended) A vertical transistor as recited in claim 2, further including

a contact formed in an opening in said isolation material adjacent said [insulating material] insulator to a conductive region at an end of said pillar.

6. (Amended) An integrated circuit device including

isolation material surrounding transistor locations in a substrate,

vertical field effect transistors formed at said transistor locations and having a gate electrode structure formed in a trench,

a layer of insulator material in said [trenches] trench between said isolation material and said gate

electrode structure, said isolation material being selectively etchable relative to said layer of insulator and

a contact opening formed along an interface of said layer of insulator material and said isolation material.

8. (Amended) A device as recited in claim 6, further including

a contact formed in said contact opening in said isolation material adjacent said [insulating material] insulator and extending to a conductive region extending below said pillar.

20. (Amended) A transistor as recited in claim 18, wherein said gate structure extends on two sides of said channel.

35. (Amended) A transistor as recited in claim [32] 34 wherein said substrate comprises SOI having buried oxide isolation and wherein said insulation comprises said buried oxide isolation.